

Johan Jino

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EDUCATION

MEng Electronic and Information Engineering

Imperial College London

- On track for First Class. Achieved 77% Year 3.
- Modules of interest: Machine Learning (83%), Advanced Computer Arch (82%), Digital Systems (85%), Software Systems (76%).
- Developed ExecEngine (ANSI C compiler) for RISC-V architecture, rated second best compiler in the cohort of 150 students.
- Designed an FPGA mathematical function accelerator on Intel DE-1 SoC, which ranked top 3 in execution time.

09/2021 – 06/2025

London,
United Kingdom

All India Senior School Certificate

GEMS United Indian School

- Graduated with an average of 95.4% score overall.
- School topper for Physics (96), Mathematics (96), Chemistry (96) and Computer Science (95).

2018 – 2021

Abu Dhabi,
United Arab Emirates

PROFESSIONAL EXPERIENCE

System Software Engineer Intern

Nvidia 🔗

- Working with the Holoscan for Media team to develop software-defined Kubernetes platform for video broadcast orchestration.
- Performed Benchmarking on platform for achieve speed of light data transfer.
- Worked on system performance optimizations leveraging RDMA, GPU Direct, Multi-Instance GPU, Time Slicing, CUDA MPS.
- Improved efficiency by reducing number GPUs required by >50%, for 4K 60fps ST2110 streams while mainting compliance.
- Created custom metrics monitoring toolchain using Prometheus and Grafana for deploying applications on Kubernetes, using Helm. Pushed to production.
- Visualized hardware metrics such as GPU memory, utilization, etc as well as high-speed network metrics such as SR-IOV Network TX/RX.

04/2024 – present

Reading,
United Kingdom

Software Engineer Intern

Qualcomm

- Worked with C++ firmware on RISC-V based hardware root of trust for Snapdragon SoC.
- Added feature to allow call stack retrieval during on-device testing. Significantly reduced debugging time for testing team.
- Worked on profiling and timing analysis tool for on-device testing.
- Scaled tool from legacy TCL to Python and added new statistical features using libraries such as Matplotlib and Tkinter.

07/2023 – 09/2023

London,
United Kingdom

Research Engineer Intern

Ivy 🔗

- Worked on new open-source python library unifying ML frameworks and allowing automated code conversions.
- Worked on backend to transpile functions from one ML framework to another.
- Created unit tests using Pytest and Hypothesis allowing property-based testing. Reviewed pull-requests and issues from the community
- Worked with Pytorch, Tensorflow, Jax and Numpy.
- Latest stable release and documentation: unifyai/ivy 🔗

07/2022 – 10/2022

London,
United Kingdom

SKILLS AND AWARDS

Technical Skills

Languages:

- *Advanced:* Python | C++
- *Intermediate:* Bash | SQL | Verilog
- *Beginner:* Golang | Java

Others:

- Experience with Profiling and Benchmarking
- Linux Development on Kubernetes Cluster and Git

AWARDS

Awards

- National Academic Excellence Award - Abu Dhabi
- Prefect of the Year Award – GEMS United Indian School
- Gold Medalist for Year 12, 11 and 10 for best performance among the all students in the cohort.
- Joint Entrance Examination India (JEE) – 88.719 percentile. Qualified for Advanced (2021)

PROJECTS

ExecEngine

02/2023 – 04/2023

ANSI C Compiler

- Developed C (C90) to RISC-V assembly compiler in a pair, with full support for integer and floats, pointers, arrays, char and structs.
- Added support for most keywords including while, switch, break, continue, enum, built-in functions like sizeof as well as multiple nested and recursive functions.
- Created Bash Scripts for test automation and Yaml for GitHub automation config.
- Scored a 80% out of all the seen and unseen test cases, putting **our compiler 2nd among all 150 students**.

MazeMaster

04/2023 – 06/2023

Self-Balancing Maze Solving Rover

As a group built an autonomous bot balanced on two wheels that traverses through an artificial maze formed using white LED strips.

- Uses FPGA based Camera Module to detect lanes and beacons. Further, used RGB thresholding to identify colored beacons.
- Programmed ESP32 micro-controller in C++ to read data from FPGA using UART and to communicate between the web-app. Multi-threading used to simultaneously achieve tasks.
- ArduinoNano used to balance the rover on 2 wheels using tuned PID controller to guide stepper motors.
- Built frontend React.js based webapp for control panel. Python based backend and pathfinding algorithm built to autonomously control rover with a DynamoDB database.

RISC-V CPU

11/2022 – 12/2022

SystemVerilog CPU Design

- Designed a multi-stage pipe-lined CPU compliant to RISC-V 32-bit integer instruction set architecture in SystemVerilog.
- Built both pipelined and data cached version of the CPU
- Includes an independent C++ test-bench which can be used to assert the functional correctness of any given CPU.
- GitHub automation was deployed to prevent failures from creeping into main branch
- Worked on RTL Design, TestBenching, Workflow automation

OTHER SKILLS

- Writing documentation and reports in Markdown and LaTeX
- Experience with Agile and DevOps methodologies
- Worked with scrum project management system and used tools like Workfront, Workday, and Monday.
- Completed Goldman Sachs Engineering Virtual Program.
- Extracurriculars & Hobbies: Volunteering, Badminton, learning new medicinal and scientific findings.
- Badminton World Federation (BWF) International Series Selectee - Representing UAE.
- Excellent PowerPoint skills, including morph transitions for 3D Models.